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(71) Applicants
James Alexander Carter
25 Harlech Close, West Durrington, West Sussex, United Kingdom

David Jeffery Carter
Flat 7, 66 South Terrace, Littlehampton, West Sussex, United Kingdom

(72) Inventors
James Alexander Carter
David Jeffery Carter

(74) Agent and/or Address for Service
Frank B Dehn & Co
Imperial House, 15-19 Kingsway, London, WC2B 6UZ, United Kingdom

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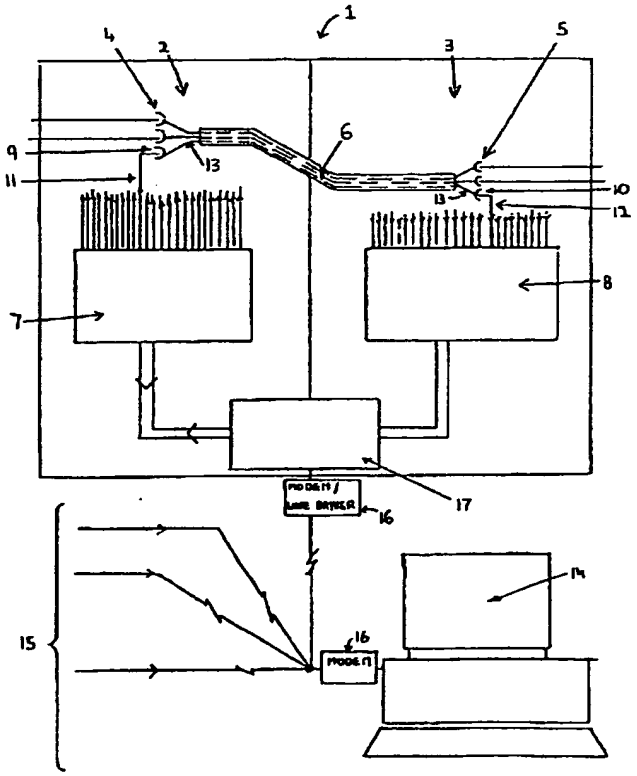
(54) Self documenting patch panel

(57) In a method for documenting the connections (6) between input and output ports (4,5) of a patch panel (1) wherein each port has a polling terminal (9, 10) associated with it, a polling signal is sent (7) in turn, to each of the input polling terminals (9) of the input ports, and the output ports whose polling terminals (10) receive the signal are identified (8, 17, 14) as being connected to that input port. The sending circuitry (7) includes serial parallel shift registers (18 Fig 2 not shown) and the receiving circuitry (8) includes parallel to serial shift registers (19).

Figure 1



The claims were filed later than the filing date within the period prescribed by Rule 25(1) of the Patents Rules 1982.

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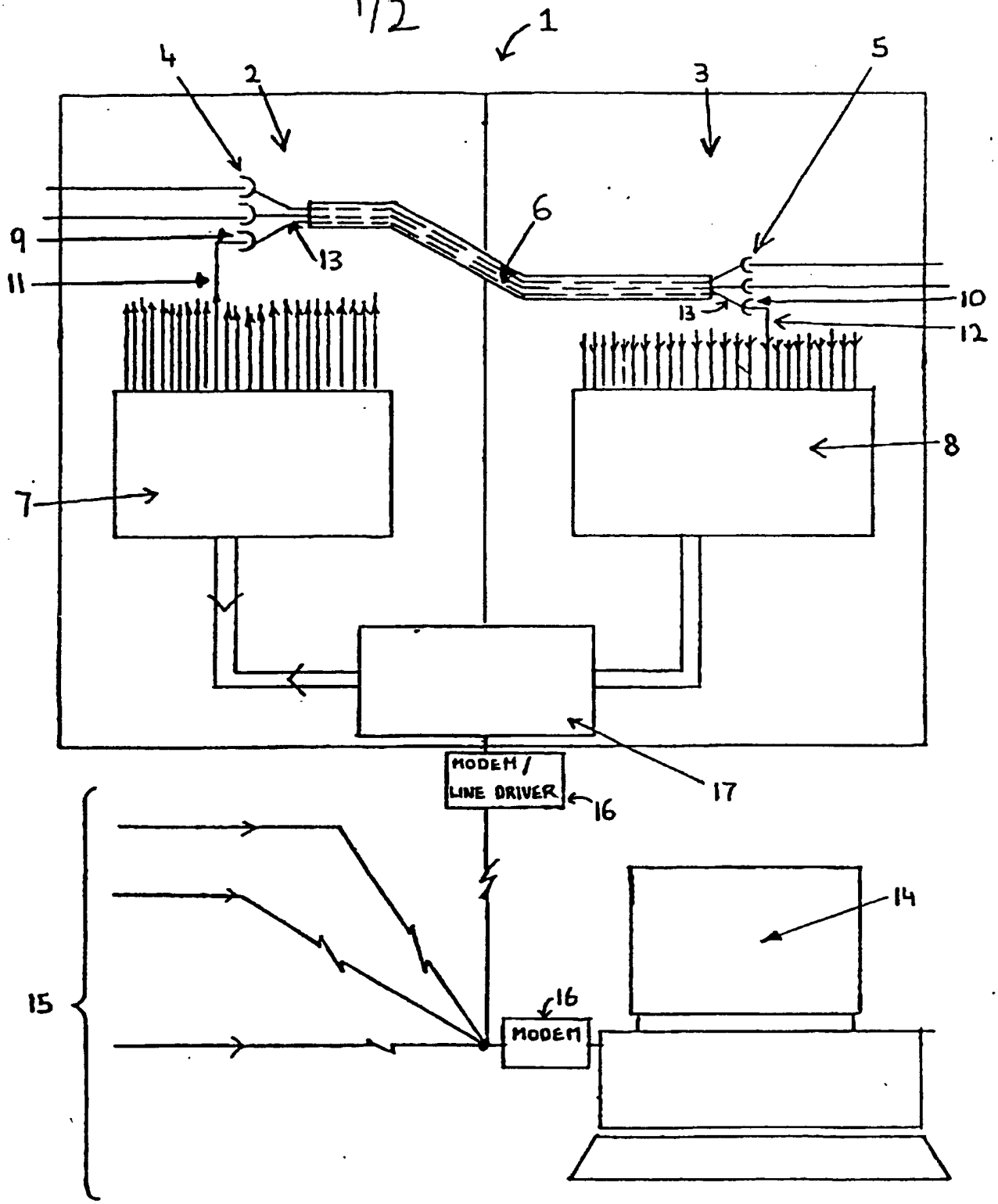

Figure 1

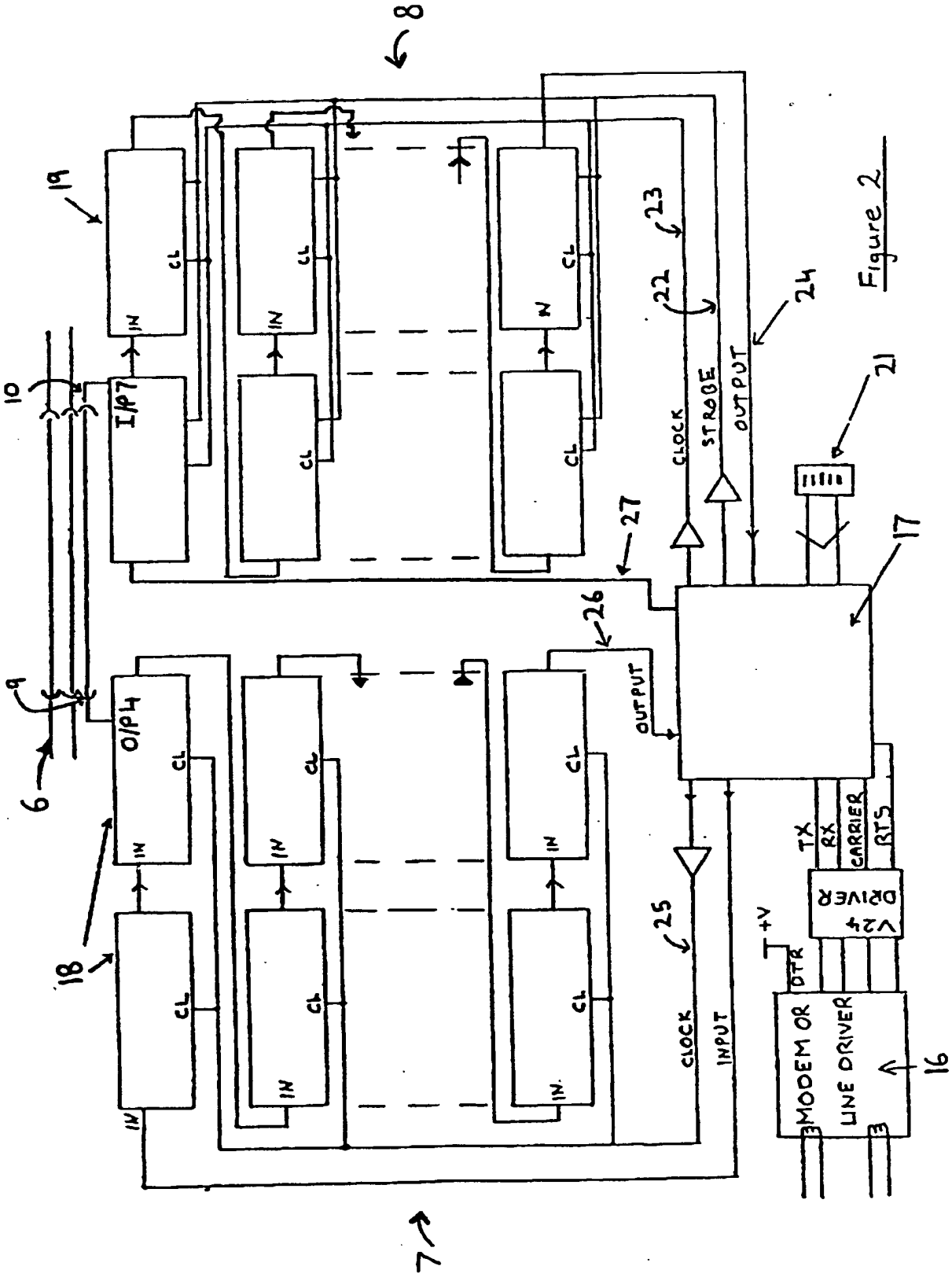
8
19
CL
IN
I/P 7
10
9
6
O/P 4
18
7
26
OUTPUT
27
CLOCK
STROBE
OUTPUT
23
22
24
21
17
25
CLOCK
INPUT
TX
RX
CARRIER
RTS
DRIVER
+V
DTR
MODEM OR
LINE DRIVER
16

Figure 2

Self Documenting Patch Panel

This invention relates to patch panels.

A patch panel (distribution frame or wiring frame) is used in wiring systems to enable changes to the wiring to be made easily. A patch panel consists of two groups of ports, which may be a group of input ports and a group of output ports, for example. For a connection to be made between an input port and an output port a patch lead is used to join the two ports.

Designers of wiring systems are making more frequent use of patch panels; and patch panels, particularly in modern office blocks, are becoming larger and more complex. At present, the connections made through a patch panel are documented manually. This documentation is therefore time consuming, and liable to be inaccurate and/or out of date.

It is an object of the present invention to provide a method and apparatus for automatically documenting the connections made on a patch panel. This enables the precise paths of all cables to be known, aids fault diagnosis and could automatically point out capacity problems in the cabling system.

Viewed from one aspect, the invention provides a method of documenting the connections made between a first set of ports and a second set of ports of a patch panel, comprising the steps of: providing each of the first set of ports with an input polling terminal, providing each of the second set of ports with an output polling terminal, connecting an input polling terminal to an output polling terminal when the corresponding port of

the first set of ports is connected to the corresponding port of the second set of ports, sending a polling signal to each of the input polling terminals in turn, detecting at which output polling terminal(s) the polling signal is received, and associating each port of the second set of ports having a so-detected output polling terminal with the port of the first set of ports having the input polling terminal polled. The first and second sets of ports may be input and output ports of the patch panel, respectively, or vice versa, for example.

Preferably, a polling signal is sent to each of the input polling terminals in turn, and, after each signal is sent, all of the outputs of the output polling terminals are read to detect whether they have received the polling signal.

Preferably the polling signal is produced at each input polling terminal by connecting each input polling terminal to a respective output of a serial-to-parallel shift register and clocking a logical pulse across each output of the serial-to-parallel shift register in turn.

Preferably also, the output polling terminals receiving the polling signal are detected by connecting each of the output polling terminals to a respective input of a parallel-to-serial shift register, loading the inputs from the output polling terminals onto the parallel-to-serial shift register, clocking the loaded inputs along the register until they reach the output of the register, and noting the number of clock pulses taken for a logical pulse to reach this output.

Further preferably, the sending of the polling signal, the detection of the polling signal and the association of the ports of the first set of ports with the ports of

the second set of ports is controlled by a microprocessor.

The above method may also be used for documenting the connections made between the ports of each patch panel in a system of patch panels, wherein an overall controller polls each patch panel in turn, each polled patch panel then documenting the connections made between its ports using the above method and sending this information to the controller.

Viewed from a second aspect the invention provides a patch panel comprising a first set of ports and a second set of ports adapted for connection with each other by connection means, an input polling terminal associated with each port of the first set of ports, an output polling terminal associated with each port of the second set of ports, polling means for sending a polling signal to each input polling terminal, receiving means for detecting at which output polling terminals the polling signal is received, and identification means for identifying the association of each port corresponding to the so-detected output polling terminals with the port corresponding to the polled input terminal.

In use, connection means are used to connect ports of the first set each with one or more ports of the second set and the connection means simultaneously connects the corresponding input and output polling terminals.

Preferably, the polling means comprises a serial-to-parallel shift register the outputs of which are connected to the input polling terminals, means being provided for clocking a logical pulse across each output of the serial-to-parallel shift register in turn.

Preferably also, the receiving means comprises a

parallel-to-serial shift register, the inputs of which are connected to the output polling terminals, loading means for loading the input from the output polling terminals onto the parallel-to-serial shift register, clocking means for clocking the loaded inputs along the register until they reach the output of the register, and counting means for counting the number of clock pulses taken for a logical pulse to reach the output of the parallel-to-serial shift register.

Further preferably, the identification means comprises a microprocessor which also controls the polling means and receiving means.

The above apparatus may also be used in a wiring system comprising a number of the above described patch panels, wherein an overall controller is provided for polling each of the patch panels in the system, and for receiving the information as to the connections between the first and second sets of ports of the patch panels.

An embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a schematic block diagram of a system according to the invention; and

Figure 2 is a more detailed block diagram.

A patch panel 1 comprises a panel 2 for mounting a set of ports such as input port 4, and a panel 3 for mounting a set of ports such as output port 5. An example patch lead 6 is shown connecting input port 4 to output port 5.

Included in the patch panel are polling circuitry 7 and

receiving circuitry 8 which are used to determine the input and output port connections. Besides having the usual terminals, each port on the patch panel has an additional terminal 9 or 10. Each additional terminal 9 on the input side of the patch panel is wired to a unique output 11 of the polling circuitry 7. Each additional terminal 10 on the output side of the patch panel is wired to a unique input 12 of the receiving circuitry 8. Each patch lead has an additional conductor 13, which connects a unique pair of these terminals when it connects an input port to an output port. Hence, a unique pair of inputs and outputs of the polling and receiving circuitry are connected via the patch lead.

The connections made on the patch panel can be identified by the polling circuitry sequentially polling each input port and detecting whether a response is received by the receiving circuitry. The data can then be sent to a central database in an overall controller 14 via a modem or line driver 16. The controller 14 also collates information from other patch panels in the system, 15. The controller, which may be a standard computer using commercially available software, can then provide the required management reports on the patch panel connections.

Fig. 2 shows the patch panel polling circuitry, which consists principally of serial-to-parallel shift registers 18, and the receiving circuitry 8, which consists principally of parallel-to-serial shift registers 19. The microprocessor 17 controls the polling and sends the results to the overall controller via a modem or line driver 16. The outputs of the serial-to-parallel shift registers 18 are connected to the additional terminals 9 of the input ports 4 of the patch panel 1. The inputs of the parallel-to-serial

shift registers 19 are connected to the additional terminals 10 of the output ports 5 of the patch panel 1. The example patch lead 6 connects output port 4 of the second serial-to-parallel shift register to input port 7 of the first parallel-to-serial shift register 19.

Each patch panel is given a unique address which is set by a switch 21.

The overall controller 14 contains a record of the input/output port connections of all of the patch panels. Where no connection exists for an input port 4 then this should also be denoted, e.g. by zeros. It should be noted that a port on the input side of the patch panel may be connected to more than one port on the output side of the patch panel. An example record is shown in Table 1.

Patch Panel "27"

Port (Input Side)	Port (Output Side)
001	007
002	100
003	512, 027
004	000
...	...
...	...
775	531

TABLE 1

The database in the overall controller 14 will hold this information for each patch panel in the system.

When the database is to be updated, the controller 14

polls each patch panel 1 in turn. When a patch panel is polled the patch panel's microprocessor 17 interrogates the patch panel 1. To do this, the microprocessor 17 loads a logical one into the first bit of the first serial-to-parallel shift register 18. This allows connections to input port one of the input side of the patch panel to be determined.

The microprocessor 17 instructs a load of all the inputs from the output polling terminals to the parallel-to-serial shift registers 19 by activating a strobe signal on line 22. The microprocessor 17 then shifts the data out of the registers 19 by a clock pulse on line 23 and samples it for logical ones, via line 24. The number of clock signals required to receive each logical one is recorded and each number is related directly to the port number of each of the output ports to which input port one is connected.

The microprocessor 17 sends the results for port one to the controller 14. The controller 14 then stores the data in the appropriate file for the patch panel 1.

The microprocessor now clocks the serial-to-parallel registers 18 via line 25 so that the logical one is moved to the second output port of the shift register 18 to enable connections for input port two to be tested. The process then continues as for input port one.

The process is repeated as above for all other outputs of the serial-to-parallel shift registers 18.

The controller 14 then polls all the other patch panels in the system.

To facilitate error checking of the patch panel electronics, on either the input or the output side of

the patch panel, the microprocessor should check that a logical one is received back on line 24 or 26, as appropriate, after the correct number of clock cycles. For the purposes of checking the output side electronics a test signal is provided on line 27.

Although the patch panel has been described as having a set of input and output ports, it will be appreciated that information may flow in either direction between the ports. Also, the input polling terminals and output polling terminals could be on the output ports and input ports respectively, instead of, as described, on the input ports and output ports respectively.

Claims:

1. A method for documenting the connections made between a first set of ports and a second set of ports of a patch panel, comprising the steps of: providing each of the first set of ports with an input polling terminal, providing each of the second set of ports with an output polling terminal, connecting an input polling terminal to an output polling terminal when the corresponding port of the first set of ports is connected to the corresponding port of the second set of ports, sending a polling signal to each of the input polling terminals in turn, detecting at which output polling terminal(s) the polling signal is received, and associating each port of the second set of ports having a so-detected output polling terminal with the port of the first set of ports having the input polling terminal polled.

2. A method as claimed in claim 1, wherein said first set of ports are input ports and said second set of ports are output ports.

3. A method as claimed in claim 1 or 2, wherein a polling signal is sent to each of the input polling terminals in turn, and, after each signal is sent, all of the outputs of the output polling terminals are read to detect whether they have received the polling signal.

4. A method as claimed in claim 1, 2 or 3, wherein the polling signal is produced at each input polling terminal by connecting each input polling terminal to a respective output of a serial-to-parallel shift register and clocking a logical pulse across each output of the serial-to-parallel shift register in turn.

5. A method as claimed in any preceding claim, wherein

the output polling terminals receiving the polling signal are detected by connecting each of the output polling terminals to a respective input of a parallel-to-serial shift register, loading the inputs from the output polling terminals onto the parallel-to-serial shift register, clocking the loaded inputs along the register until they reach the output of the register, and noting the number of clock pulses taken for a logical pulse to reach this output.

6. A method as claimed in any preceding claim, wherein the sending of the polling signal, the detection of the polling signal and the association of the ports of the first set of ports with the ports of the second set of ports is controlled by a microprocessor.

7. A patch panel comprising a first set of ports and a second set of ports adapted for connection with each other by connection means, an input polling terminal associated with each port of the first set of ports, an output polling terminal associated with each port of the second set of ports, polling means for sending a polling signal to each input polling terminal, receiving means for detecting at which output polling terminals the polling signal is received, and identification means for identifying the association of each port corresponding to the so-detected output polling terminals with the port corresponding to the polled input terminal.

8. A patch panel as claimed in claim 7, wherein the polling means comprises a serial-to-parallel shift register the outputs of which are connected to the input polling terminals, means being provided for clocking a logical pulse across each output of the serial-to-parallel shift register in turn.

9. A patch panel as claimed in claim 7 or 8, wherein

the receiving means comprises a parallel-to-serial shift register, the inputs of which are connected to the output polling terminals, loading means for loading the input from the output polling terminals onto the parallel-to-serial shift register, clocking means for clocking the loaded inputs along the register until they reach the output of the register, and counting means for counting the number of clock pulses taken for a logical pulse to reach the output of the parallel-to-serial shift register.

10. A patch panel as claimed in claim 7, 8 or 9, wherein the identification means comprises a microprocessor which also controls the polling means and receiving means.

11. A wiring system, comprising a plurality of patch panels according to any of claims 7 to 10.

12. A wiring system as claimed in claim 11, wherein an overall controller is provided for polling each of the patch panels in the system, and for receiving the information as to the connections between the first and second sets of ports of the patch panels.

13. A method of documenting the connections made between a first set of ports and a second set of ports of a patch panel, substantially as herein described with reference to the accompanying drawings.

14. A patch panel, substantially as herein described with reference to the accompanying drawings.

15. A wiring system, substantially as herein described with reference to the accompanying drawings.

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